

## A POWER EFFICIENT MULTIPLIER ARCHITECTURE FOR FIR FILTERS USED FOR ACOUSTIC MODELS IN MECHANICAL DIAGNOSTICS

R. MANIKANDAN, K.HARIHARAN & VENKATESAN. R

School of Computing, Sastra University, Thanjavur, Tamil Nadu, India

### ABSTRACT

*Finite Impulse Response (FIR) channels are broadly utilized as a part of multi standard remote interchanges. The important pre requisites of channels are re configurability and low many-sided quality. This paper proposes effective consistent multiplier (CM) engineering in light of vertical even parallel regular sub expression disposal calculation for planning a reconfigurable FIR (Finite Impulse Response) channel. In channel, the product function is computed between the input and constants coefficients defined as the multiple constant multiplication (MCM). At long last this Multiplication procedure is connected on to the Common reconfigurable FIR channel as the application improvement. Due to this proposed sub expression elimination, the number of addition stage in the multiplication process and the repeated additions were reduces, and also the logic utilization of the device reduced when compared to the existing multiplication process. Power consumption also less when compared to the full multiplication process. The proposed result shows the efficiency of the novel architecture submitted. This paper shows an acoustical model for control and diagnostics of single stage adapt wheels. The model depends on different strategies and methods that accordingly give data about the generator's condition, the rigging specifically. The acoustical model is a piece of an unpredictable framework that units' distinctive models to meet diagnostics of single stage outfit wheels as exact as could be expected under the circumstances. Utilizing the versatile FIR channel, acoustical model empowers the count of motivation reaction for various indent lengths in the vicinity of 0 and air conditioning. The acoustical model comprises of computerized FIR channel, changed by LMS calculation, used to compute motivation reactions in non-straight frameworks, Recurrence range of the reenacted sound flag empowers an examination of the blunder that can be utilized for computing the rest of the administration life and additionally deciding the control cycle of support.*

**KEYWORDS:** Constant Multiplier, Finite Impulse Response & Multiple Constant Multiplications

**Received:** Sep 19, 2017; **Accepted:** Oct 09, 2017; **Published:** Nov 14, 2017; **Paper Id.:** IJMPERDDEC201735

### INTRODUCTION

Filter channels is broad usage in portable correspondence frameworks for applications example, channel evening out, coordinated separating, because of their supreme solidness, straight stage applications. The channels utilized as a part of versatile frameworks must be acknowledged to expend less power and work at rapid. The many-sided quality of channels commanded through the intricacy of constant multiplier is notable the common sub expression elimination (CSE) techniques in view of accepted marked digit constant deliver low multifaceted nature filter channel constant multiplier. Coefficients. Multifaceted nature of multipliers coefficient can be diminished in consolidating strategies. It offers a decent tradeoff amongst LD and LOs, especially for higher request channels. The multiplier is the significant imperative which characterizes the execution of the desired channel, thus the point VLSI configuration is to decrease the parameters like area, power, and speed. By decreasing the exchanging exercises of the multiplier in Fir channel the many-sided quality will be diminished

and henceforth territory will likewise get lessen. To plan the productive consistent multiplier the common sub expression disposal strategies is utilized. The Binary CSE (BCSE) calculation manages end of excess parallel regular sub expression that happens inside the coefficients. The numbers of adders to implement the BCSE for coefficient multiplier is less than the CSD-based CSE methods.

## RECONFIGURABLE CHANNEL ARCHITECTURE

Reconfigurable channel designs are proposed for low power and area executions to acknowledge different recurrence reactions utilizing a solitary digital filter. For low power designs, variable input word-length and number of channel taps, diverse coefficient word-lengths, and element minimized flag representation procedures are utilized. In those works, vast overhead is brought about to bolster reconfigurable plans, for example, self-assertive nonzero digit task or programmable move.

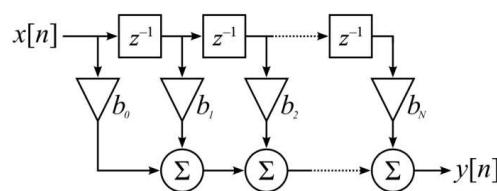


Figure 1: FIR Channel Direct Form

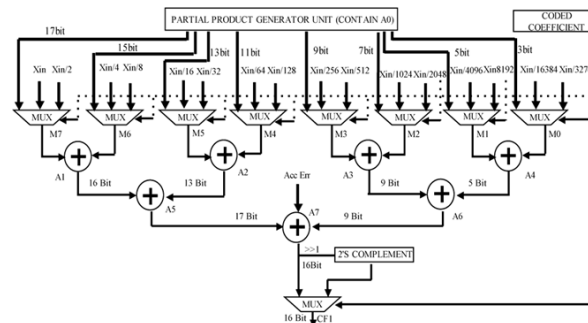
In Figure.1, weighted estimations of info successions are summed up in the FIR Channel operation is called as conventional sum. These are as often as possible used to execute determination of recurrence, for example, low-pass, high-pass, or band-pass channels. For the most part, the consequence of summation and its related force of FIR channel are straightforwardly corresponding to the channel arrange. algorithm. The main advantage of the method is without changing the architecture we can implement this technique.

## BCSE ALGORITHM, ISSUES AND PROPOSED SOLUTION

The flat BCSE count utilizes CSs occurring inside each coefficient to discard monotonous figuring's, VBCSE uses basic sub expression transversely over close-by constants to get rid of overabundance estimations. According to BCSE computation an entirety of  $2n - (n+1)$ . The sub expression are obtained from a  $n$ -bit common elements and the summers need to form  $2n-1 - 1$ . In this method the coefficients are changed dynamically. In this method the result of frequently appearing group of bits can be used for upcoming similar bits. Hence the computation can be reduced in this BCSE. The FBCSE algorithm is used in previous works. The different problem performed in reconfigurable filter used in a part of multi standard DUC is the part of SDR/intellectual radio. To reduce the power and area performance by using the VLSI design of an intermediate filter for DUC. This paper(1) uses 2-bit BCSE for more efficient but there are some issues in that are mentioned as below: It consists of two type of architectures coefficient and signed magnitude. the signed magnitude method is used for the data representation it obtain certain different in architecture for considering wide application. These methods apply the algorithm only in the first layer (A0-A7) and adder is used for the sum of partial products generated. The MAT used for the partial product addition is ignored by this method.

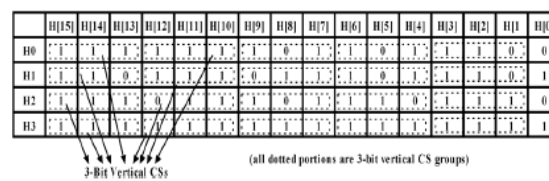
The proposed algorithm is used to solve the above mentioned issues: The coefficient of filter is convoluted between the complemented and original format based on the MSB of the coefficient. it reduced the complexity of hardware. The proposed algorithm is applied in layer-1 of 2-bit BCSE vertically and 4-bit,8-bit of horizontally I the rest of

layers by obtaining the common expression in the coefficient. it also reduces hardware by reducing the common sub expressions. And also MAT in different layer of 2, 4, 8-bit will optimize the area and power utilization for higher level synthesis.

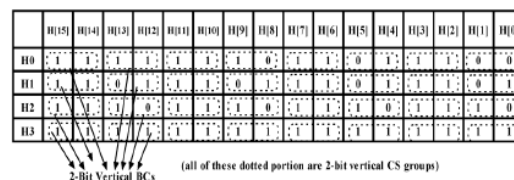


**Figure 2: Reconfigurable Filter using 2-Bit BCSE**

In paper (1) the algorithm is applied only on the first layer of the block diagram and the remaining layers are executed as an addition of normal layer so the area and power will be consumed a lot to overcome this issues the algorithm of VHBCSE is applied on the each and every layer till the final output execution. The algorithm is applied as a 2-bit BCSE and 3-bit BCSE the example of using this in a 8-Tap symmetric FIR filter.



**Figure 3: Tap FIR Filter by using 3-Bit BCSE**

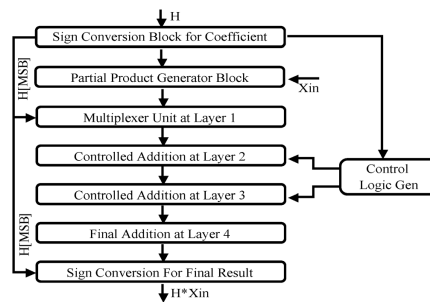


**Figure 4: Tap FIR Filter by using 3-Bit BCSE**

## PROPOSED METHOD

The VHBCSE calculation based consistent multiplier VHBCSE utilizes 2-bit BCSE vertically to the adjoining constants, trailed from 8 to 4-bit level CSEs to distinguish and kill whatever number BCSs as could reasonably be expected which are available inside each of the coefficient. Our changed calculation computed marked number for the info and the coefficients alongside lessened likelihood to utilization of the summers (A0-A7) to aggregate up the halfway item generator. The dataflow graph for the proposed VHBCSE calculation is as per the following. The composed multiplier considers the length individually need the yield is thought must be 16-bit size. The tested data sources were used before the coefficients in LUTs in the enlist. In this paper the VHBCSE algorithm is implemented in the multiplier that is used in FIR filter and this is compared with the FIR filter with array multiplier for the area and for the delay. In normal array multiplier all the partial products are computed each and every time. Due to this the switching activity of the multiplier is increased and power consumption is increased to overcome this CSE method is used. In our work calculation, a 2-bit vertical BCSE

is connected to the neighboring constants, continued by other level BCSEs to distinguish thus take out however lot of BCSs as could be expected under the circumstances which are available inside each of the coefficient.



**Figure 5: Data Flow Diagram**

### ALGORITHM STEPS

The proposed algorithm for vertical horizontal binary common sub expression elimination algorithm has some procedure to be follow and it uses the 3-bit to be replaced by 2-bit.

- Obtain the 16bit as input xin [15:0]
- The input is then stored in a coefficient (c [16:0]) of length 17-bit in lookup table
- The input is then converted by taking 1's complement (c' [15:0]).
- The MSB of the input 17<sup>th</sup> bit is used as a select signal to choose the input in normal format(c[15:0]) or in complemented format(c'[15:0]) to produce the multiplexed coefficient.
- The multiplexed coefficient is then partitioned into 2-bit of each and used as a select line for multiplexer (M0-M7).
- The MC is now partitioned into 4-bit of each (mc [15:12], mc [11:8], mc [7:4], mc [3:0])
- The partitioned MC, mc [15:12] with mc [11:8] is now in the next layer. If it matches A2 step is skipped and replaced by (4-bit shifted right) A1 for the input of A5 otherwise use the output of A2.
- The partitioned MC mc [15:12] with mc [7:4] in 2<sup>nd</sup> layer is now in the next layer. If it matches A3 step is skipped and replaced by (8-bit shifted right) A1, for the input of A6 otherwise mc[11:8] with mc[7:4] in 2<sup>nd</sup> layer is now in the next layer. If it matches A3 step is skipped and replaced by (4-bit shifted right)A2 for the input of A6 otherwise use the output of A3
- The MC mc [15:12] with mc [3:0] in 2<sup>nd</sup> layer is now in the next layer. If it matches, A4 step is skipped and replaced by (12-bit shifted right) A1, for the input of A6, otherwise mc [11:8] with mc [3:0] in 2<sup>nd</sup> layer is now in the next layer. If, it matches A4 step is skipped and replaced by (8-bit shifted right) A2, for the input of A6 otherwise the MC mc [7:4] with mc [3:0] in 2<sup>nd</sup> layer is now in the next layer. If, it matches A4 step is skipped and replaced by (4-bit shifted right) A3 for the input of A6 use the output of A3.
- The MC is then subdivided into the group of mc[15:8],mc[7:0]
- MC mc [15:8] with mc [7:0] is now in the 3rd layer. If it matches A6 step is skipped and replaced by (8-bit shifted

right) A5 for the input of A7 otherwise use the output of A5.

- The final result of addition is shifted by 1-bit right side as A7.
- The output A7 is obtained after 2's complement.
- If the MSB of 17<sup>th</sup> bit is 1 then the complemented format are chosen otherwise the normal format is choose for the final result A7.
- Now the algorithm is completed and the result is stored in a c\*x in the register

## ARCHITECTURE

- **Sign Conversion Block:** This block will support both the input and coefficient in signed data representation. The design of this block is as shown in Fig. It has the one's complement design to produce the opposite result of coefficient. The 16-bit 2:1 multiplexer will generate the multiplexed coefficient with respect to the MSB of coefficient.

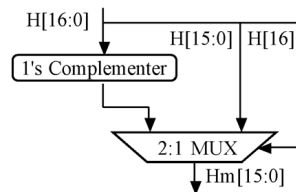


Figure 6: Design of Sign Conversion Block

- **B) Partial Product Generator (PPG):** This design is to use for basic shifting and summer operation to obtain the products and after that those are summed to the upcoming levels to produce the output.



Figure 7: Design of the Partial Product Generator Unit

- **Multiplexers Unit:** This block is used for the selection of corresponding data generated from PPG block with respect to coefficient binary value. Based on 2-bit BCSE this algorithm is used in vertically on Multiplier Adder Tree (MAT). The multiplexer used in this with the width of 17, 15, 13, 11, 9, 7, 5, and 3-biteach instead of 16-bit for all, by this way the power and area will consumed
- **Control Logic (CL) Generator:** This block is used to generate the 7 control signals based on the various different test vectors.

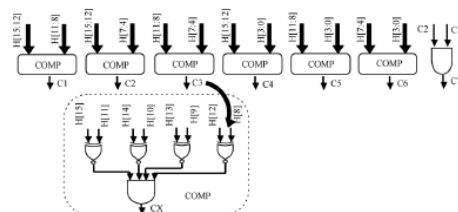


Figure 8: Control Logic Generator Unit

- **Controlled Layer-2:** The product obtained from previous level is summed to get the final result that is computed in these levels. It needs four additions for eight products. The control signal is used as select lines for adders. This level reduces PPGs.

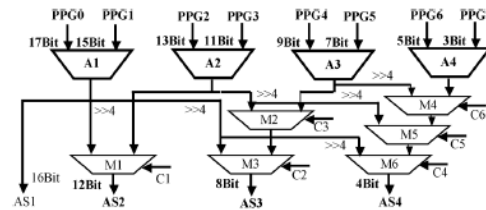


Figure 9: Layer-2 Block

- **Addition Layer-3:** The result of previous layers is used in blocks. The last signal is used to generate the two addition result from four inputs instead of direct summation.

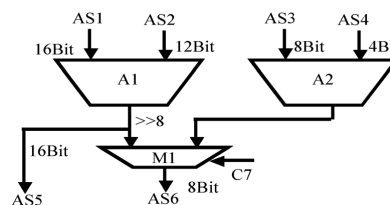


Figure 10: Controlled Addition at Layer-3

- **Layer-4 Summation:** This design is used to obtain the final result of multiplication from the summation performed between the two sums.

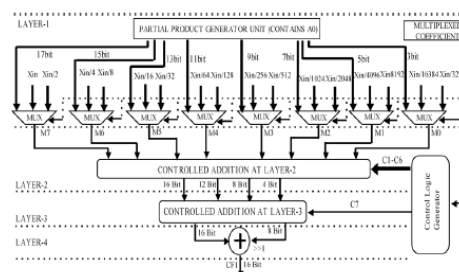


Figure 11: Proposed Architecture

## RESULTS AND DISUSSIONS

The VHBCSE calculation based steady multiplier design, has been coded utilizing Verilog equipment depiction dialect. The reproduction comes about for the proposed structure for filters 16-bit length. Thus the multiplier used in filter using VHBCSE algorithm is compared with the normal array multiplier used filters for area and delay consumptions.

	Map	
FIRclk	S01	
FIRrst	S00	
FIRN	1001110001011010	
FIRsel	01	
FIRN4	1111111111111111	
FIRN3	1111111111111111	
FIRN2	1111111111111111	
FIRN1	1111111111111111	
FIRN	000000000000000010010111111111110011	

Figure 12: FIR using VHBCSE Algorithm

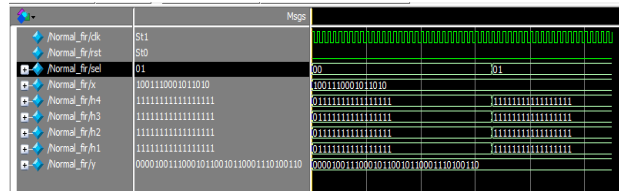


Figure 13: FIR using Normal Array Multiplier

The simulation is for the computation of a both input by using the normal array multiplier implemented in the simulation tool modelsim. By using VHBCSE, the power consumption is comparatively lesser than normal array multiplier.

## PERFORMANCE COMPARISONS

Table I: Power Consumptions

	Multiplier Implemented VHBCSE Algorithm	Using Normal Array Based Multiplier
Thermal Power	135.82mw	144.49mw
Static Power	78.55mw	98.50mw

Table II: Parameters Consumptions

parameters	Multiplier Implemented VHBCSE Algorithm	Using Normal Array based Multiplier
Input LUT's	13%	77%
Delay	26.882 ns	45.141 ns

## CONCLUSIONS

In this paper an underlying common sub expression can be evacuated by applying another vertical-horizontal BCSE calculation in vertically 2-bit BCSE. Encourage transfer of the sub expressions are done by grouping the CSs appear inside the constants by performing BCSs to unique sizes effectively not in any manner like level of the move then incorporate due to unflinching multiplier outline. Subsequently the outcome has been demonstrated that the proposed strategy lessens the sensible component usage and power utilization when looked freely customary channel technique. The proposed half breed type of VHBCSE multiplier reconfigurable structures gave low Power and Area.

## REFERENCES

1. I. Hatai, I. Chakrabarti, and S. Banerjee, "An efficient VLSI architecture of a reconfigurable pulse-shaping FIR interpolation filter for multi-standard DUC," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, May 2014 [Online]. Available: <http://ieeexplore.ieee.org>
2. R. Mahesh and A. P. Vinod, "A new common subexpression elimination algorithm for realizing low-complexity higher order digital filters," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 27, no. 2, pp. 217–229, Feb. 2008
3. Mohsen Amiri Farahani, Eduardo Castillo Guerra, Bruce G. Colpitts, "Efficient implementation of fir filters based on a novel common Subexpression elimination algorithm", *IEEE Conference Publications*, 1 - 4, DOI: 10.1109/CCECE.2010.5575223, 2010
4. Smitha. K. G and A. P. Vinod, "A New Binary Common Subexpression Elimination Method for Implementing Low Complexity FIR Filters", *IEEE Conference Publications*, 2327 - 2330, DOI: 10.1109/ISCAS.2007.378854, 2007.

5. Vijay, s. and Vinod, A. P. (2007) "A Greedy Common Subexpression Elimination Algorithm for Implementing FIR Filters ", *IEEE 1-4244-0925-7/07...*,
6. Vijay, s. and Vinod, A. P. (2007) "A Greedy Common Subexpression Elimination Algorithm for Implementing FIR Filters ", *IEEE 1-4244-0925-7/07...*,
7. R. Pasko, P. Schaumont, V. Derudder, S. Vernalde, and D. Durackova, "A new algorithm for elimination of common subexpressions," *IEEE Trans. Comput.-Aided Design Integr. circuits Syst.*, vol. 18, no. 1, pp. 58–68, Jan. 1999.
8. M. M. Peiro, E. I. Boemo, and L. Wanhammar, "Design of high-speed multipliersless filters using a nonrecursive signed common subexpression algorithm," *IEEE Trans. Circuits Syst. II*, vol. 49, no. 3, pp. 196–203, Mar. 2002.
9. Mateja Ploj Vrtič, Boris Aberšek, Uroš Župerl, "Using of Acoustic Models in Mechanical Diagnostics," *Journal of Mechanical Engineering* 54(2008)12, 874-882